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				Application Number	10/734708
				Filing Date	
				First Named Inventor	Visokay et al.
				Group Art Unit	2813
Examiner Name					
Sheet	1	of	1	Attorney Docket No.	TI-35227

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
TSP	AA	5,352,623		Kamiyama	10/04/1994	Entire Document
	AB	5,891,809		Chau et al.	04/06/1999	Entire Document
	AC	6,013,553		Wallace et al.	01/11/2000	Entire Document
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	AN	6,624,090	B1	Yu et al.	09/23/2003	Entire Document
	AO	2003/0080389	A1	Hu et al.	05/01/2003	Entire Document
TSP	AO	2003/0129817	A1	Visokay et al.	07/10/2003	Entire Document

FOREIGN PATENT DOCUMENTS							
Exam. Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS				
Exam. Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
TSP	CA	"Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications", SEIJI INUMIYA, KATSUYUKI SEKINE, SHOKO NIWA, AKIO KANEKO, MOTOYUKI SATO, TAKESHI WATANABE, HIRONOBU FUKUI, YOSHIKI KAMATA, MASATO KOYAMA, AKIRA NISHIYAMA, MARIKO TAKAYANAGI, KAZUHIRO EGUCHI and YOSHITAKA TSUNASHIMA, 2003 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.		
	CB			

Examiner Signature		Date Considered	10/14/05
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